

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes formed on the surface thereof;

an interposer substrate on which said semiconductor chip is mounted;

a core substrate constituting the base of said interposer substrate;

built-up layers built on only one surface of said core substrate;

an anisotropic conductive layer which is formed on the other surface of said core substrate, and via which said semiconductor chip is mounted on said core substrate; and

the electrodes on said core substrate and those on said semiconductor chip being electrically connected via said anisotropic conductive layer.

2. A semiconductor device in accordance with claim 1, wherein each of the built-up layers built on said core substrate has an elastic modulus of 5000 MPa or below.

3. A semiconductor device in accordance with claim 1, wherein said core substrate is formed of a material having an elastic modulus closer to that of said semiconductor chip

than to that of said built-up layer.

4. A semiconductor device in accordance with claim 1, wherein each of said built-up layers has curved wiring patterns formed on the surface thereof so as to relax stress.

5. A semiconductor device in accordance with claim 1, wherein said core substrate is formed of a material having a thermal expansion coefficient closer to that of said semiconductor chip than to that of said built-up layers, and wherein said core has a thickness of 0.5 mm or below.

6. A semiconductor device in accordance with claim 1, wherein, on the core substrate surface on which said built-up layers are built, reinforced patterns are formed at the positions corresponding to the electrodes on said semiconductor chip.

7. A semiconductor device in accordance with claim 6, wherein said interposer substrate is constructed by forming built-up layers on said core substrate, wherein electrodes are each formed so as to be continuous with a conductive portion which passes through said built-up layer, and wherein said electrodes are connected to the motherboard to be affixed thereon.

8. A semiconductor device in accordance with claim 7, wherein, on the outer surface of said built-up layer, no wiring patterns exist at the positions corresponding to said reinforced patterns, and wherein through-holes are formed at the corresponding positions on the motherboard to mount said semiconductor device.

9. A method for manufacturing a semiconductor device by mounting a semiconductor chip on an interposer substrate, said method comprising:

preparing an interposer substrate by forming built-up layers on one surface of a core substrate;

mounting said semiconductor chip, via an anisotropic conductive layer, on the other surface opposite to said one surface on which said built-up layers of said core substrate have been formed; and

electrically connecting the electrodes on said semiconductor chip and those on the other surface of said core substrate via said anisotropic conductive layer.

10. A method for manufacturing a semiconductor device in accordance with claim 9, wherein a plurality of built-up layers is successively formed on the one surface of said core substrate.

11. A method for manufacturing a semiconductor device in accordance with claim 9, wherein holes are formed in said built-up layers, wherein the surface of said built-up layers including said holes are plated with a conductive metal, and wherein wiring patterns and vias are simultaneously formed on said built-up layers by etching said plated layers.

11. A method for manufacturing a semiconductor device in accordance with claim 9, wherein holes are formed in said built-up layers, wherein the surface of said built-up layers including said holes are plated with a conductive metal, and wherein wiring patterns and vias are simultaneously formed on said built-up layers by etching said plated layers.